# Reset from Multiple Power Supplies

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Processor based systems usually require a voltage supervisor chip to produce a clean reset pulse to the processor whenever a ‘brown-out’ condition of the power supply is detected. More complex designs employing multiple power supplies can be unreliable if some of the supplies are not supervised. The circuit described here monitors all the supply rails in the system (here +12 V, –12 V and +5 V) and provides a reset pulse to the processor whenever it detects any are not within tolerance.

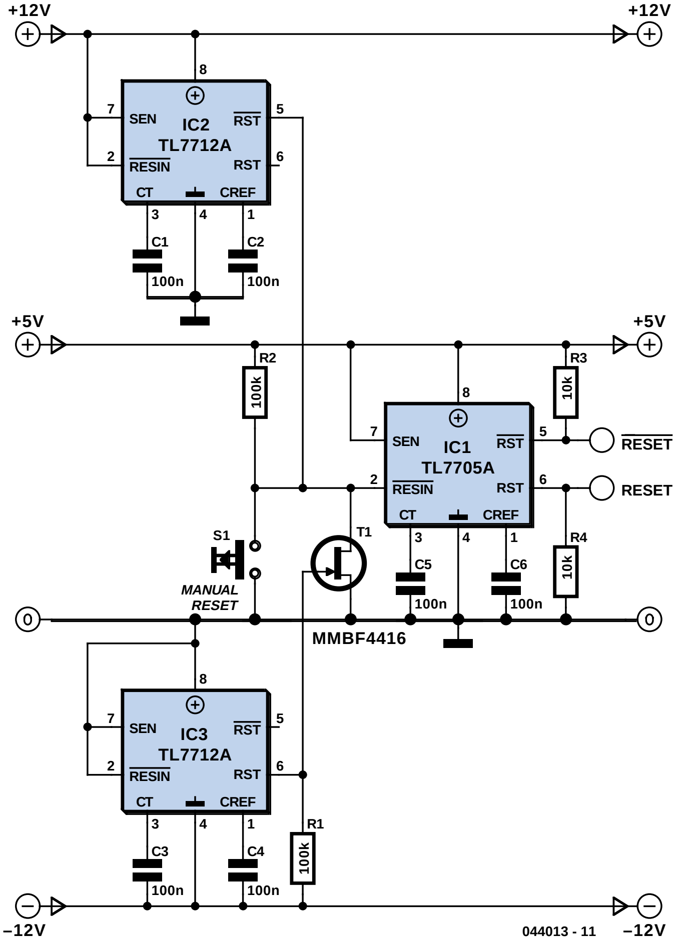
IC1 (TL7705A) generates a processor reset if the 5 V rail falls below 4.55 V. The value of the capacitor fitted to pin 3 defines the reset pulse width $t_d$ according to the formula:

$$t_d = 12 \cdot C_T \cdot 10^3$$

With $C_T$ in μF the value for $t_d$ is given in μs. A capacitor of 100 nF for example, will produce a reset pulse of around 1.2 ms. Pin 6 (RESET) outputs an active-high pulse and Pin 5 ($\overline{\text{RESET}}$) an active-low pulse. The outputs are open collector types so an external pull-down and pull-up resistor (respectively) is required.

The $\overline{\text{RESIN}}$ input (Pin 2) of IC1 is driven from two TL7712A supervisors monitoring +12 V (IC2) and –12 V (IC3). The TL7712A generates a reset when the supply voltage falls below a threshold level of 10.8 V. The open collector output $\overline{\text{RES}}$ (Pin 5) of IC2 is connected to the $\overline{\text{RESIN}}$ pin of IC1 and pulled up to 5 V via a 100 kΩ resistor. The open collector output of IC2 can be directly connected to the reset input of IC1 but the output of IC3 must be connected via a level shifting device before it can be connected to the reset input of IC1 because the voltage level at the output of IC3 goes negative. JFET transistor T1 is used to perform the necessary level shifting. The JFET turns off when the voltage at its gate-source junction is between –2.5 V and –6 V. When IC3 is issuing a reset signal the RES output (pin 6) will go up to ground potential and cause T1 to conduct and trigger a reset of IC1. At all other times the RES output of IC3 will be pulled to a minus voltage via the 100 kΩ resistor which then causes T1 to stop conducting and release the reset. A manual reset push button can also be connected to $\overline{\text{RESIN}}$ of IC1 if required. The SENSE input (Pin 7) of the TL77xx chips is connected to the positive supply rail. The reference input (pin 1) is fitted with a 100 nF capacitor to reduce the effects of fast transients.

The JFET type MMBF4416 is available from Conrad Electronic (www.conrad.de), order no. 14 28 08



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